UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/580,755	05/30/2000	Hong Wang	884.225US1	1888

21186 7590 06/17/2005

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. BOX 2938
MINNEAPOLIS, MN 55402-0938

EXAMINER	
MEONSKE, TONIA L	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 06/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/580,755	WANG ET AL.	
	Examiner	Art Unit	
	Tonia L. Meonske	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7-9,11 and 31-67* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *3,38 and 61* is/are allowed.

6)☒ Claim(s) *1, 2, 4, 5, 7-9, 11, 31-37, 39-60,and 62-67* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

2. The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 33-34 are rejected under 35 U.S.C. 102(b) as being anticipated by Asghar et al., U.S. Patent Number 5,794,068 (herein referred to as Asghar).

4. Referring to claim 33 Asghar has taught a method comprising:

a. Loading a first stream of instructions containing essential code into a first memory (Asghar figures 1 and 4, numbers 202, 102, 212, 214, abstract, column 4 lines 11-67);

b. Loading a second stream of instructions containing non-essential code into a separate second memory (Asghar figure 4, number 444, abstract, column 10 lines 45-64;

the data cache holds the operands for the DSP functions and the results, so part of the second instruction steam must go there to be stored);

c. Storing a mapping table relating a plurality of triggers to respective ones of a plurality of different sequences of the non-essential code, where each trigger includes at least one of a plurality of different conditions resulting from execution of essential code (Asghar figures 8 and 10, abstract, column 3 line 61-column 4 line 11, The actual code is the trigger which specifies the conditions for instruction execution.);

d. Executing instructions from the essential code from the first memory in a microarchitecture structure until detecting an occurrence one of the triggers (Asghar figures 1 and 3, abstract, column 4 lines 11-67); and

5. Thereafter, executing instructions from one of the non-essential code sequences in the same microarchitecture structure, the one sequence being specified by the at least one condition of the one trigger (Asghar figures 1 and 3, abstract, column 4 lines 11-67; in figure 1 both the GP CPU and the DSP are shown in the same CPU).

6. Referring to claim 34 Asghar has taught wherein the first and second memories are first and second pipelines (Asghar figure 4 abstract, column 4 lines 11-67).

7. Claims 1-2, 4-5, 7-9, 11, 31-33, 35-37, 39-60, and 62-67 rejected under 35 U.S.C. 102(e) as being anticipated by Jones et al., U.S. Patent Number 6,745,222 (herein referred to as Jones).

8. Referring to claim 1 Jones has taught a processor comprising a first memory configured to store a sequence of instructions representing essential code (Jones column 2 lines 4-24, column 2 lines 33-49; it is essential that the group of instruction in a real-time thread be executed by a deadline);

a. a second memory configured to store a sequence of instructions representing non-essential code (Jones column 2 lines 4-24, column 21 lines 5-17; it is not essential that the non-real time threads are executed by a deadline); and

b. a conjugate mapping table configured with a plurality of triggers to relate different sequences of the non-essential code to respective contingent conditions that specify predefined attributes of the essential code (Jones column 7 line 33-column 8 line 13, column 5 line 47-column 7 line 13, abstract, column 20, line 51-column 21, line 28, The precomputed schedules and constraints are the predefined attributes as claimed.); and

c. a single microarchitecture structure configured to execute instructions both from the essential code and from the non-essential code, the processor being coupled to both the first and second memories to process code from the first memory, and to process code from the second memory in response to the triggers (Jones column 6 lines 5-8).

2. Referring to claim 2 Jones has taught wherein the first memory is coupled to a first instruction cache configured to cache instructions that determine the logical correctness of a program (Jones column 2 lines 4-24, column 5 lines 64-67, Column 20, line 51-column 21, line 28).

3. Referring to claim 4 Jones has taught wherein the first memory is coupled to registers that store a micro architectural state, and wherein the conjugate mapping table is responsive to the microarchitectural state (Jones column 2 lines 4-24, column 7 line 33-column 8 line 13).

4. Referring to claim 5 Jones has taught further comprising:

a. a first instruction cache coupled to the first memory (Jones column 2 lines 4-24, column 5 lines 64-67; each of the threads have there own space in memory; both threads are stored in cache systems); and

b. a second instruction cache coupled between the conjugate mapping table and the second memory (Jones column 2 lines 4-24, column 5 lines 64-67; each of the threads have there own space in memory).

2. Referring to claim 7 Jones has taught wherein the conjugate mapping table comprises a plurality of records, each of the plurality of records being configured to map a trigger to a non-essential code sequence (Jones column 7 line 33-column 8 line 13, column 5 line 47-column 7 line 13 column 22 lines 37-45).

3. Referring to claim 8 Jones has taught wherein the trigger comprises an atomic value, such that the conjugate mapping table is configured to specify the non-essential code sequence when the atomic value is satisfied (Jones column 7 line 33-column 8 line 13, column 5 line 47-column 7 line 13 column 22 lines 37-45).

4. Referring to claim 9 Jones has taught wherein the trigger comprises a vector value, such that the conjugate mapping table is configured to specify the non-essential code sequence when the vector value is satisfied (Jones column 7 line 33-column 8 line 13, column 5 line 47-column 7 line 13 column 22 lines 37-45).

5. Referring to claim 11 Jones has taught wherein the microarchitectural structure includes a register bank (Jones column 2 lines 4-24, column 2 lines 33-49).

6. Referring to claim 31 has taught further comprising a dynamic code analyzer to generate non-essential code from the essential code in the first memory (Jones column 6 lines 11-27).

7. Referring to claim 32 has taught further comprising a dynamic code analyzer directed acyclic graph trace representations of at least some of the essential code from the first pipeline (Jones column 6 lines 11-27).

8. Referring to claim 33 Jones has taught a method comprising:

a. Loading a first stream of instructions containing essential code into a first memory (Jones column 2 lines 4-24, column 2 lines 33-49; it is essential that the group of instruction in a real-time thread be executed by a deadline);

b. Loading a second stream of instructions containing non-essential code into a separate second memory (Jones column 2 lines 4-24, column 21 lines 5-17; it is not essential that the non-real time threads are executed by a deadline);

c. Storing a mapping table relating a plurality of triggers to respective ones of a plurality of different sequences of the non-essential code, where each trigger includes at least one of a plurality of different conditions resulting from execution of the essential code (Jones column 7 line 33-column 8 line 13, column 5 line 47-column 7 line 13, Column 20, line 51-column 21, line 28, There are a plurality of different possible times for the plurality of different stored timing constraints.);

d. Executing instructions from the essential code from the first memory in a microarchitecture structure until detecting an occurrence one of the triggers (Jones column 7 line 33-column 8 line 13, column 5 line 47-column 7 line 13; the scheduler makes the switch based on the priorities and constraints, and is predetermined); and

2. Thereafter, executing instructions from one of the non-essential code sequences in the same microarchitecture structure, the one sequence being specified by the at least one condition of the one trigger (Jones column 6 lines 5-8).

3. Referring to claim 35 Jones has taught wherein the first and second memories are caches (Jones column 2 lines 4-24, column 5 lines 64-67; each of the threads have there own space in memory; both threads are stored in cache systems)

4. Referring to claim 36 Jones has taught wherein the first and second memories are logically separate (Jones column 2 lines 4-24; the threads are kept separate and have their own space).

5. Referring to claim 37 Jones has taught wherein the first and second memories are physically separate (Jones column 2 lines 4-24; the threads are kept separate and have their own space).

6. Referring to claim 39 Jones has taught wherein the non-essential code includes sequences to perform instruction set virtualization (Jones column 2 lines 4-24, column 2 lines 33-49).

7. Referring to claim 40 Jones has taught wherein the included sequences perform respectively multiple ones of the functions (Jones column 2 lines 4-24, column 2 lines 33-49).

8. Referring to claim 41 Jones has taught wherein certain of the essential code is stored in the second memory (Jones column 2 lines 4-24, column 2 lines 33-49).

9. Referring to claim 42 Jones has taught wherein the certain essential code includes sequences for virtualization (Jones column 2 lines 4-24, column 2 lines 33-49).

10. Referring to claim 43 Jones has taught wherein at least one of the sequences virtualizes one or more entities selected from the group consisting of: individual instructions, blocks of

instructions, sets of register, and processor hardware resources (Jones column 2 lines 4-24, column 2 lines 33-49).

11. Referring to claim 44 Jones has taught where the triggers are instruction attributes (Jones column 7 line 33-column 8 line 13, column 5 line 47-column 7 line 13; the time constraints are related to the instructions of the thread, so they are instruction attributes).

12. Referring to claim 45 Jones has taught where the instructions attributes include opcodes, locations, and/or operands (Jones column 7 line 33-column 8 line 13, column 5 line 47-column 7 line 13; the time constraints are associated with certain threads in certain locations).

13. Referring to claim 46 Jones has taught wherein the data attributes include values and/or locations (Jones column 7 line 33-column 8 line 13, column 5 line 47-column 7 line 13).

14. Referring to claim 47 Jones has taught wherein the state attributes include architectural and/or microarchitecutal states (Jones column 2 lines 4-24, column 2 lines 33-49).

15. Referring to claim 48 Jones has taught wherein the event attributes include interrupts, exceptions, and/or processor state register values (Jones column 7 line 33-column 8 line 13, column 5 line 47-column 7 line 13; the constraints are held in registers).

16. Referring to claim 49 Jones has taught a system comprising:

a. storage to have a single library having

b. a first part containing instructions representing essential code for executing a particular program (Jones column 2 lines 4-24, column 2 lines 33-49; it is essential that the group of instruction in a real-time thread be executed by a deadline) and

c. a second part containing sequences of instructions representing nonessential code associated with the same particular program (Jones column 2 lines 4-24, column 21 lines

5-17; it is not essential that the non-real time threads are executed by a deadline), wherein the non-essential code includes code generated from the essential code (Merriam-webster's online dictionary defines "generate" as to define by the application of one or more rules. The real time threads apply timing rules that effect both essential and non-essential codes. The real time, essential code generates the timing constraints of the non-essential code.);

d. A processor including:

i. First and second memories to store the essential and non-essential code respectively (Jones column 2 lines 4-24)

ii. A mapping table to relate a plurality of triggers to a plurality of sequences of the non-essential code (Jones column 7 line 33-column 8 line 13, column 5 line 47-column 7 line 13),

iii. A single microarchitecture structure coupled to the memories to execute at least some of both the essential code and the sequences of nonessential code in response to their respective triggers (Jones column 6 lines 5-8).

2. Referring to claim 50 Jones has taught wherein the memory includes at least one cache (Jones column 2 lines 4-24, column 5 lines 64-67).

3. Referring to claim 51 Jones has taught wherein the memory includes one or more of a hard disk, a floppy disk, RAM, ROM, a flash memory, and/or a medium readable by a machine (Jones column 7 line 33-column 8 line 13).

4. Referring to claim 52 Jones has taught where the memory stores the essential and non-essential code in separate sections of a file (Jones column 2 lines 4-24).

5. Referring to claim 53 Jones has taught where the essential and nonessential code reside in a static file (Jones column 2 lines 4-24).

6. Referring to claim 54 Jones has taught where the nonessential code resides at least partly in a run-time library (Jones column 2 lines 4-24).

7. Referring to claim 55 Jones has taught where the single microarchitecture structure is configured to execute all instructions from both the essential and the non-essential code (Jones column 7 line 33-column 8 line 13, column 5 line 47-column 7 line 13);).

8. Referring to claim 56 Jones has taught wherein the second pipeline further contains some code that is not essential (Jones column 2 lines 4-24, column 21 lines 5-17, column 2 lines 33-49).

9. Referring to claim 57 Jones has taught wherein the non-essential code includes sequences to perform interrupt or exception processing (Jones column 2 lines 4-24, column 21 lines 5-17, column 2 lines 33-49).

10. Referring to claim 58 Jones has taught wherein the non-essential code includes sequences to perform speculative execution (Jones column 2 lines 4-24, column 21 lines 5-17, column 2 lines 33-49).

11. Referring to claim 59 Jones has taught wherein the non-essential code includes sequences to perform security checking or sandboxing (Jones column 2 lines 4-24, column 21 lines 5-17, column 2 lines 33-49).

12. Referring to claim 60 Jones has taught wherein the non-essential code includes sequences to test the microarchitecture (Jones column 2 lines 4-24, column 21 lines 5-17, column 2 lines 33-49).

13. Referring to claim 62 Jones has taught wherein at least one of the sequences virtualizes blocks of instructions (Jones column 2 lines 4-24, column 21 lines 5-17, column 2 lines 33-49).

14. Referring to claim 63 Jones has taught wherein at least one of the sequences virtualizes sets of registers (Jones column 2 lines 4-24, column 21 lines 5-17, column 2 lines 33-49).

15. Referring to claim 64 Jones has taught wherein at least one of the sequences virtualizes processor hardware resources (Jones column 2 lines 4-24, column 21 lines 5-17, column 2 lines 33-49).

16. Referring to claim 65 Jones has taught where the triggers are data attributes (Jones column 7 line 33-column 8 line 13, column 5 line 47-column 7 line 13).

17. Referring to claim 66 Jones has taught wherein the triggers are state attributes (Jones column 7 line 33-column 8 line 13, column 5 line 47-column 7 line 13).

18. Referring to claim 67 Jones has taught wherein the triggers are event attributes (Jones column 7 line 33-column 8 line 13, column 5 line 47-column 7 line 13).

Response to Arguments

19. Applicant's arguments with respect to claims 1-5, 7-9, 11, 31-67 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

20. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

21. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

22. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L. Meonske whose telephone number is (571) 272-4170. The examiner can normally be reached on Monday-Friday, 8-4:30.

23. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P. Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

24. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

tlm

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100